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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,310	09/11/2003	Richard L. Coulson	ITL.1029US (P16765)	5388

21906 7590 12/14/2004

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EXAMINER	
BHAT, ADITYA S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,310	COULSON ET AL.	
	Examiner	Art Unit	
	Aditya S Bhat	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,13-16,21,26-28 and 33-45* is/are rejected.

7)☒ Claim(s) *4-6,8,10-12,17-25 and 29-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 7, 13-16, 21, 26-28, 33-45 rejected under 35 U.S.C. 102(b) as being anticipated by Lamb et al. (USPN 6,662,136).

With regards to claim 1 and 13, Lamb et al. (USPN 6,662,136) teaches a method comprising, or an article comprising a medium storing instructions that, if executed, enable a processor based system to

monitoring the temperature of a cache memory; (Col.1, lines 7-11) and

in response to a detection of a temperature condition, transitioning the cache memory from a write-back cache to a write-through cache. (Col.5, lines 33-65)

With regards to claim 2, 27-28, 40-41 and 44 Lamb et al. (USPN 6,662,136) teaches monitoring the temperature of a ferroelectric polymer cache memory. (10,20;Figure 1)

With regards to claim 3, Lamb et al. (USPN 6,662,136) teaches adjusting the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transitioning the cache from a write-back cache to a write-through cache. (Col.5, lines 11-65).

With regards to claim 7and 16, Lamb et al. (USPN 6,662,136) teaches shutting off the said cache memory at a temperature above said second temperature.(Col.2, lines 30-31)

With regards to claim 9, Lamb et al. (USPN 6,662,136) teaches upon detecting a lower temperature, resuming operation of said cache memory. (Col.5, lines 11-17)

With regards to claim 14, Lamb et al. (USPN 6,662,136) teaches storing instructions that, if executed, enable a processor-based system to monitor the temperature of a ferroelectric polymer cache memory. (Col. 1, lines 7-11)

With regards to claim 15, Lamb et al. (USPN 6,662,136) teaches storing instructions that, if executed, enable a processor-based system to adjust the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transition the cache memory from a write-back to a write-through cache. (Col.5, lines 11-65)

With regards to claim 26, Lamb et al. (USPN 6,662,136) teaches a processor-based system comprising:

a processor; (30;figure 1)

a disk drive coupled to said processor; (10, 20;figure 1)

a cache memory coupled said processor; (10,20;figure 1)and

a storage to store a cache driver to monitor the temperature of said cache memory and in response to the detection of a temperature condition, transition the cache memory from a write-back cache memory to a write-through cache memory. (Col.5, lines 33-65)

With regards to claim 33, Lamb et al. (USPN 6,662,136) teaches a storage stores instructions that enable the system to resume cache operations after shutting off the cache memory in response to a cache condition by initially resuming reduced speed operations in a first stage and thereafter resuming normal operations. (Col. 2, lines 30-31)

With regards to claim 34, Lamb et al. (USPN 6,662,136) teaches cache memory includes a temperature sensor. (Col.1, line 7)

With regards to claim 35, Lamb et al. (USPN 6,662,136) teaches a circuit comprising:

a component to receive an indication of the temperature of a cache memory and to develop a signal to transition the cache memory from a write-back cache to a write-through cache in response to said temperature indication. (Col.5, lines 11-65)

With regards to claim 36, Lamb et al. (USPN 6,662,136) teaches a component to vary the operation of a system to adjust for the temperature affected operation of said cache memory. (Col. 2, lines 30-31)

With regards to claim 37, Lamb et al. (USPN 6,662,136) teaches a component to adjust a caching operation of the system in response to a temperature indication from said memory. (Col. 2, lines 30-31)

With regards to claim 38-39, Lamb et al. (USPN 6,662,136) teaches a component to shut off said cache in response to a temperature indication. (Col.2, lines 30-31)

With regards to claim 42, Lamb et al. (USPN 6,662,136) teaches cache memory includes a temperature sensor.(Col. 1,lines 7-11)

With regards to claim 43, Lamb et al. (USPN 6,662,136) teaches an integrated circuit comprising: a ferroelectric polymer memory array; and a temperature sensor. (Col.1, lines 7-11)

With regards to claim 44, Lamb et al. (USPN 6,662,136) teaches array is a cache memory. (Col.1, lines 7-11)

With regards to claim 45, Lamb et al. (USPN 6,662,136) teaches array is a disc cache memory. (Col.1, lines 7-11)

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter: Claims 4-6, 8, 10-12, 17-25 and 29-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Alexander et al. (USPN 6,029,006) teaches a data processor with circuit for regulating instruction throughput while powered method of operation, and Mittal et al. (USPN 5,719,800) teaches performance throttling to reduce IC power consumption.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aditya Bhat
December 8, 2004

John Barlow
Supervisory Patent Examiner
Technology Center 2800